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101511208

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau(43) International Publication Date
23 October 2003 (23.10.2003)

PCT

(10) International Publication Number
WO 03/088037 A1(51) International Patent Classification⁷: G06F 9/38, 9/30

(21) International Application Number: PCT/IB03/01364

(22) International Filing Date: 1 April 2003 (01.04.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
02076524.4 18 April 2002 (18.04.2002) EP

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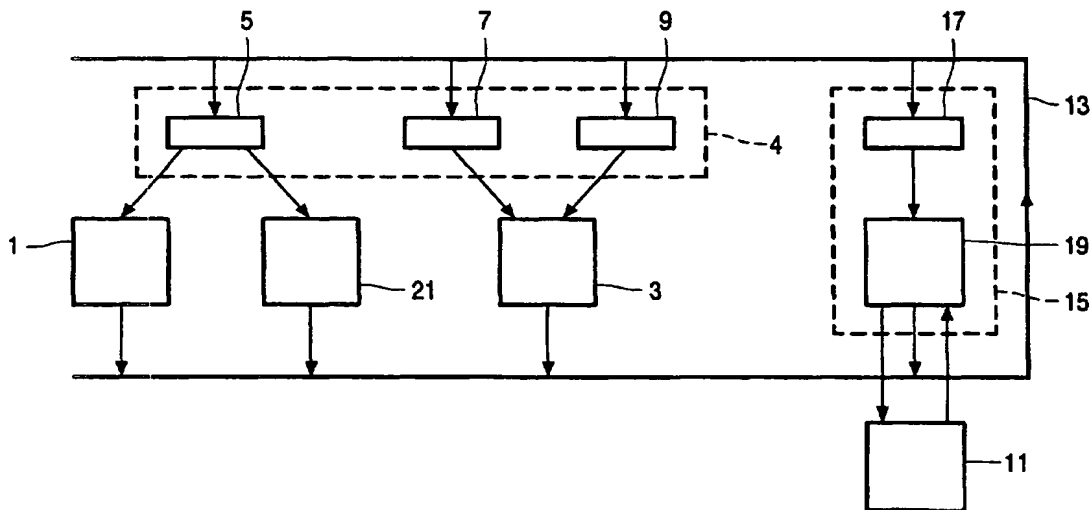
(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: VLIW PROCESSOR WITH DATA SPILLING MEANS



(57) Abstract: A VLIW processor comprising: a plurality of functional units (1, 3); a distributed register file (4) comprising a plurality of segments (5, 7, 9), the distributed register file (4) being accessible by the functional units (1, 3); a communication unit (11) for communication with a memory; a communication network (13) for coupling the functional units (1, 3) and the distributed register file (4); characterized in that the VLIW processor further comprises a spilling device (15) for transferring data between the distributed register file (4) and the communication unit (11).

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VLIW PROCESSOR WITH DATA SPILLING MEANS

TECHNICAL FIELD

The present invention relates to a VLIW processor comprising: a plurality of functional units; a distributed register file comprising a plurality of segments, the distributed register file being accessible by the functional units; a communication means for
5 communication with a memory; a communication network for coupling the functional units and the distributed register file.

BACKGROUND ART

An embodiment of the VLIW processor of the kind set forth is disclosed in
10 WO 00/33178.

A Very Long Instruction Word (VLIW) processor allows exploiting instruction-level parallelism in programs and thus executing more than one instruction at a time. A VLIW processor uses multiple, independent functional units to execute multiple operations in parallel. VLIW processors package multiple functional unit operations into one
15 very long instruction.

Limitations of VLIW processing include limited hardware resources, limited parallelism and a large increase in code size. Limited hardware resources may be the functional units, the register file or the communication network. Anticipating these limitations by adding more resources has some serious drawbacks. For example, when
20 increasing the number of functional units, the memory size and register file bandwidth will have to increase as well. Furthermore, a large number of read and write ports are necessary for accessing the register file, imposing a bandwidth that is difficult to support without a large cost in the size of the register file and degradation in clock speed.

For some applications to be run on the VLIW processor the limiting hardware
25 resource may be the register file. A large register file could be used to prevent this. However, this has several drawbacks. First, a register file with many registers may create critical timing paths and therefore limit the cycle time of the processor. Second, as the number of directly addressable registers increases, the number of bits to specify the multiple registers within the

instruction increases as well. Third, a register file with many registers occupies a large silicon area.

DISCLOSURE OF INVENTION

5 An object of the invention is to provide a VLIW processor architecture, which prevents the register file being the limiting hardware resource.

 This object is achieved with a VLIW processor of the kind set forth characterized in that the VLIW processor further comprises spilling means for transferring data between the distributed register file and the communication means.

10 It is to be noted that spilling itself is known, but from a completely different field of technology, viz. from compiler technology. The principle is that when a compiler is generating machine code and there are more live variables than the machine has registers, some variables are transferred or "spilled" from registers to memory.

 The spilling means have the capability to transfer values from the register file
15 to the communication means, via the functional units. The spilling means also have the capability to restore values by transferring them from the communication means to the register file.

 An embodiment of the invention is characterized in that the spilling means comprise a spill register file and a spill unit, the spill register file being accessible by the spill
20 unit. An advantage of this embodiment is that it prevents that the speed of transferring values by the spilling means to the communication means limits the clock frequency of the processor.

 An embodiment of the invention is characterized in that at least one of the segments of the distributed register file is associated with a functional unit that is unable to
25 pass data from the segment of the distributed register file to the spilling means, a pass unit being associated with the functional unit for passing data from the segment of the distributed register file to the spilling means. In case a functional unit, such as a ROM unit, is not able to pass the value that has to be spilled from the register file, the pass unit is capable of doing so.

30 An embodiment of the invention is characterized in that the communication network comprises a partially connected communication network. An advantage of this embodiment is that it reduces the overhead of a fully connected network.

An embodiment of the invention is characterized in that the pass unit is part of the associated functional unit. An advantage of this embodiment is that no separate pass unit is required, saving additional silicon area and communication connections.

5 BRIEF DESCRIPTION OF THE DRAWING

The features of the described embodiments will be further elucidated and described with reference to the drawing:

The single figure is a schematic diagram of a VLIW processor in accordance with an embodiment of the present invention.

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DESCRIPTION OF PREFERRED EMBODIMENTS

Referring to the figure, a schematic block diagram illustrates a VLIW processor comprising a plurality of functional units including functional units 1 and 3. The processor has a distributed register file 4 including register file segments 5, 7 and 9. The functional unit 1 can read from register file segment 5. The functional unit 3 can read from the register file segments 7 and 9.

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The processor includes a communication unit 11 for communication with a memory. The latter is not shown in this figure. The processor also includes a communication network 13, e.g. a bus, that couples the functional units 1 and 3, and the register file segments 5, 7 and 9.

20

Furthermore, the processor comprises a spilling device 15. The spilling device 15 and the register file segments 5, 7 and 9 are coupled via the communication network 13. The spilling device 15 and the functional units 1 and 3 are also coupled via the communication network 13. The spilling device 15 allows transferring values from the register file segments 5, 7 and 9 to the communication unit 11, via the functional units 1 and 3. Furthermore, the spilling device 15 can restore values by transferring them from the communication unit 11 to the register file segments 5, 7 and 9.

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Preferably, the spilling device 15 comprises a spill register file 17 and a spill unit 19. The spill unit 19 can read from the spill register file 17. An advantage of this embodiment is that it prevents that the speed of transferring values by the spilling device 15 to the communication unit 11 limits the clock frequency of the processor. In some embodiments, values can be temporarily stored in the spill register file 17, without passing them to the communication unit 11. From the spill register file 17, these values can be transferred to the register file segments 5, 7 and 9 by the spill unit 19. An advantage of this

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embodiment is that it prevents the time consuming actions of writing to and restoring values from the communication unit 11.

In an advantageous embodiment, the processor also has a pass unit 21. The pass unit 21 can read from the register file segment 5, and the pass unit 21 and the spilling device 15 are coupled via the communication network 13. The pass unit 21 allows passing the value that has to be spilled from the register file segment 5, in case the functional unit 1 is not capable of doing so. In some embodiments multiple pass units will be present, in other embodiments none will be present. A pass unit can be associated with a functional unit if that functional unit, e.g. a ROM unit, is not capable of passing a value from a register file segment.

In the embodiment shown in this figure, the pass unit 21 is a separate unit associated with functional unit 1. In some embodiments, the pass unit 21 can be part of the associated functional unit 1 by adding an additional operation to this functional unit that allows to pass a value from a register file segment.

The functional units can be coupled to one register file segment, as in case of the functional unit 1, or to multiple register file segments, as in case of the functional unit 3. The register file segments can be coupled to one functional unit or to multiple functional units. The degree of coupling between the register file segments and the functional units can depend on the type of operations that the functional unit has to perform.

The communication network 13 couples the functional units 1 and 3, and the register file segments 5, 7 and 9. The embodiment shown in this figure has a fully connected communication network, which means that every functional unit 1 and 3 is coupled to every register file segment 5, 7 and 9. In some embodiments the communication network 13 is partially connected, so not every functional unit 1 and 3 is coupled to every register file segment 5, 7 and 9. An advantage of a partially connected network compared to a fully connected network is that it is less expensive in terms of silicon area and it allows for a higher clock frequency of the processor.

The functional unit 1 and 3 as well as the pass unit 21 are coupled to the spilling device 15. In the embodiment shown in this figure, these couplings are part of the communication network 13. In some embodiments, one or more of these couplings may be separate.

The spilling device 15 is coupled to the register file segments 5, 7 and 9. In the embodiment shown in this figure, these couplings are part of the communication network 13. In some embodiments, one or more of these couplings may be separate.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

CLAIMS:

1. A VLIW processor comprising:

- a plurality of functional units;
- a distributed register file comprising a plurality of segments, the distributed register file being accessible by the functional units;
- 5 - communication means for communication with a memory;
- a communication network for coupling the functional units and the distributed register file;

characterized in that the VLIW processor further comprises spilling means for transferring data between the distributed register file and the communication means.

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2. A VLIW processor according to Claim 1 wherein:

the spilling means comprises a spill register file and a spill unit, the spill register file being accessible by the spill unit.

15 3. A VLIW processor according to Claim 1 wherein:

at least one of the segments of the distributed register file is associated with a functional unit that is unable to pass data from the segment of the distributed register file to the spilling means, a pass unit being associated with the functional unit for passing data from the segment of the distributed register file to the spilling means.

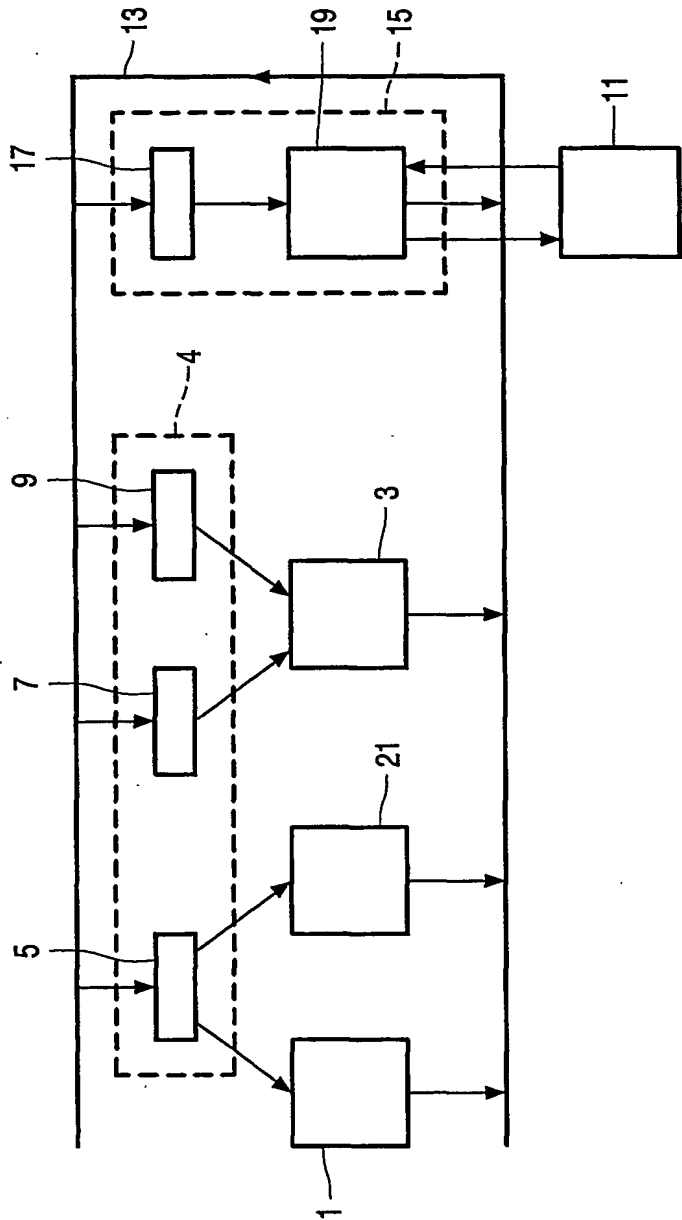
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4. A VLIW processor according to Claim 1 wherein:

the communication network comprises a partially connected communication network.

5. A VLIW processor according to Claim 3 wherein:

25 the pass unit is part of the associated functional unit.



INTERNATIONAL SEARCH REPORT

Int'l Application No

PCT/IB 03/01364

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 G06F9/38 G06F9/30

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, IBM-TDB, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 00 33178 A (SUN MICROSYSTEMS INC) 8 June 2000 (2000-06-08) cited in the application page 2, line 17 - line 19; figure 2 --- -/--	1-5

☒ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex.

* Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
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- "P" document published prior to the international filing date but later than the priority date claimed

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Date of the actual completion of the international search

30 June 2003

Date of mailing of the international search report

07/07/2003

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INTERNATIONAL SEARCH REPORT

Int'l Application No

PCT/IB 03/01364

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	<p>ZALAMEA J ET AL: "Two-level hierarchical register file organization for VLIW processors"</p> <p>MICRO-33. PROCEEDINGS OF THE 33RD. ANNUAL ACM/IEEE INTERNATIONAL SYMPOSIUM ON MICROARCHITECTURE. MONTEREY, CA, DEC. 10 - 13, 2000, PROCEEDINGS OF THE ANNUAL ACM/IEEE INTERNATIONAL SYMPOSIUM ON MICROARCHITECTURE, LOS ALAMITOS, CA: IEEE COMP. SOC, US,</p> <p>10 December 2000 (2000-12-10), pages 137-146, XP010528882</p> <p>ISBN: 0-7695-0924-X</p> <p>page 138, left-hand column, last paragraph; figure 5</p> <p>paragraphs '0004!, '05.1!</p> <p>-----</p>	1-5

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Form PCT/ISA/210 (patent family annex) (July 1992)